AL8436
4COM Segment type LCD Driver
6uA typ.

■ Features

- Fixed 1/4 duty mode, Up to 144 dots.

- Low power consumption design, 6uA current at typical condition.

- Built-in OSC Circuit

- Internal LCD Contrast control Circuit

- Integrated Power-on Reset Circuit

- No external component required

- Interface: 2 wire serial interface

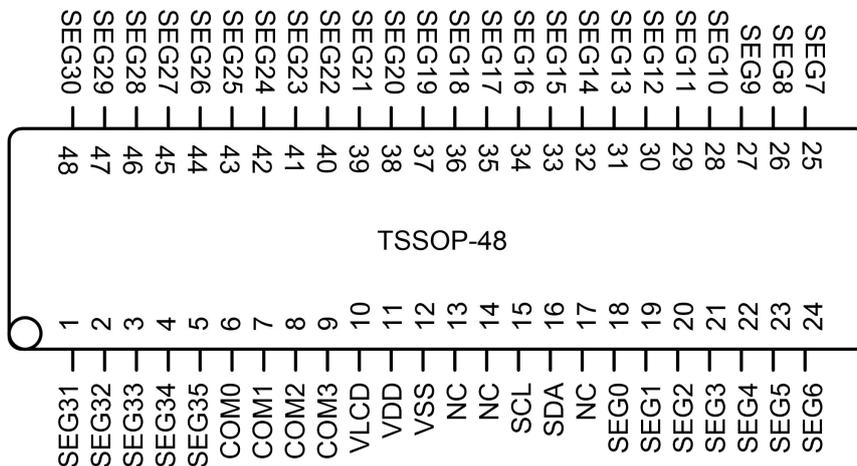- Compatible with TTL/CMOS

- High EMC immunity

■ Applications

- Home electrical appliance

- Meter equipment etc.

- Toys

- PDA

- Clocks

■ Order Information

Part No.	Package Type	Tape/Reel
AL8436	TSSOP-48	2500/Reel

■ Pin Description

Name	I/O		Function
SDA	I/O	16	2-line serial data input and output
SCL	I	15	2-line serial clock input
VSS	I	12	GND
VDD	I	11	Power supply for logic
VLCD	I	10	LCD biasing voltage, default tie low.
SEG 0~35	O	18~24,25~35,1~5	SEGMENT driver output for LCD
COM 0~3	O	6~9	COMMON driver output for LCD

# ■ Typical Application Circuit
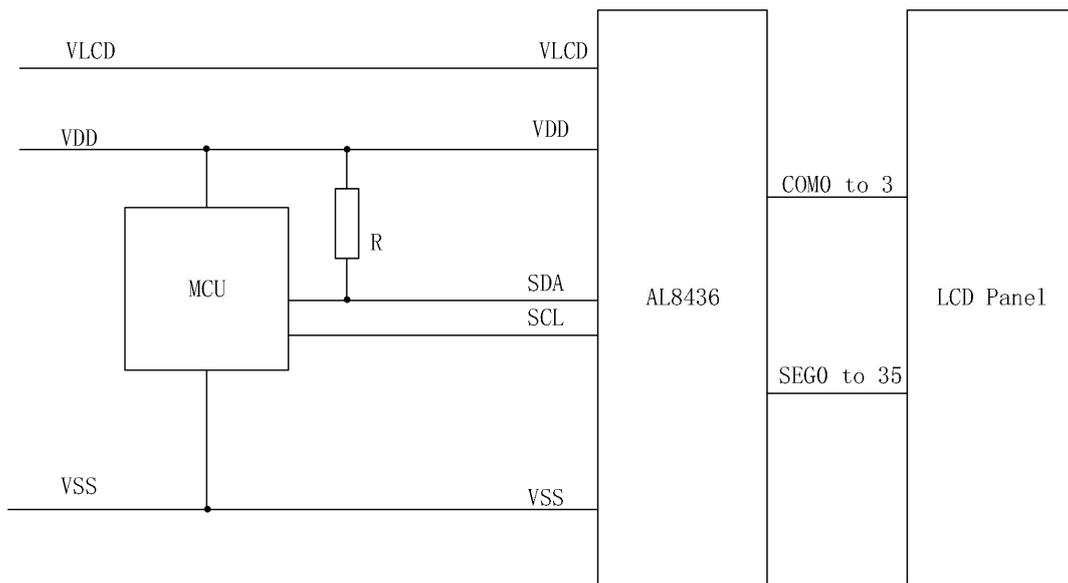
■ Block Diagram
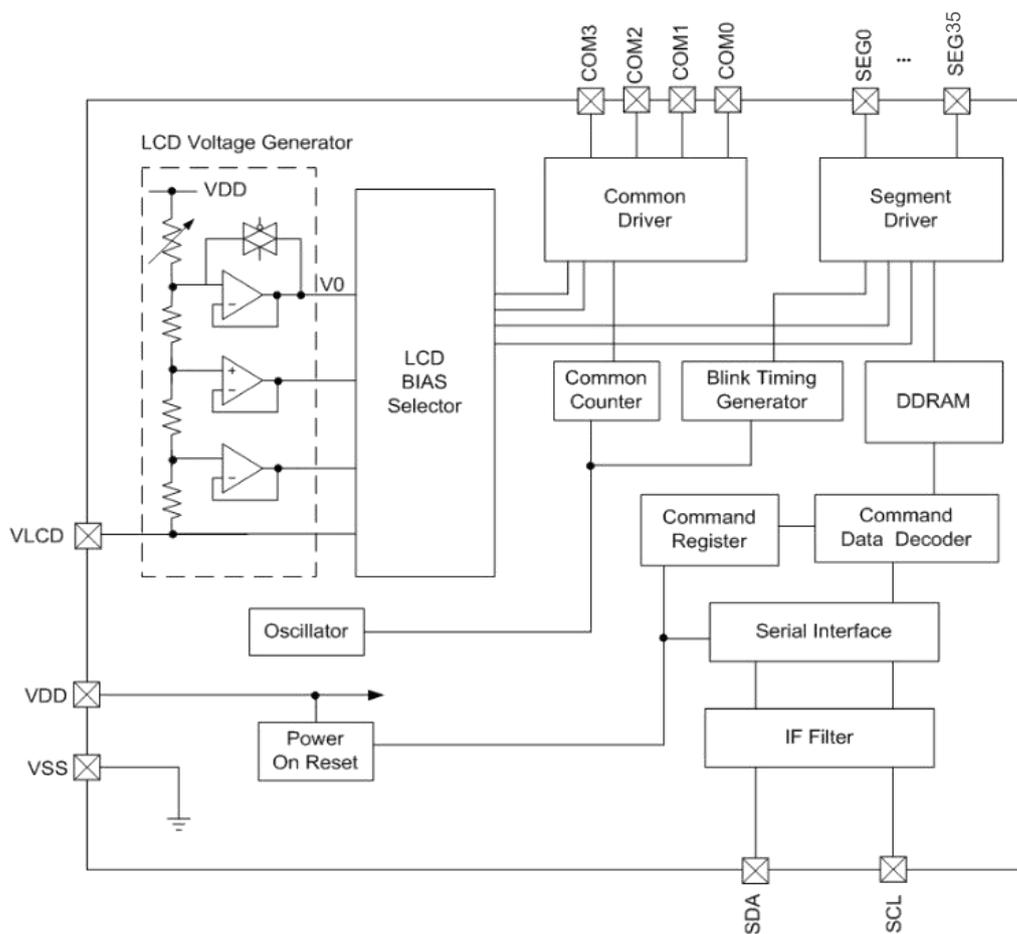
■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remarks
VDD Voltage	V_{DD}	-0.5 to + 6	V	Power supply
VLCD Voltage	V_{LCD}	-0.5 to + 0	V	LCD drive voltage
Input voltage range	V_{IN}	-0.5 to VDD + 0.5	V	
Operational temperature range	Topr	-40 to + 85	°C	
Storage temperature range	Tstg	-55 to + 125	°C	

■ Electrical Characteristics

Test conditions: VDD=3.3V, TA = 25 °C unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VDD Power Range	VDD	2.5	-	5.5		
VLCD Power Range	VLCD	-0.6	-	0	V	LCD drive voltage
"H" Level Input Voltage	VIH	0.7* VDD	-	VDD	V	
"L" Level Input Voltage	VIL	VSS	-	0.3*VDD	V	
SDA "L" Level Output Voltage	VOL_sda	0	-	0.4	V	Iload=-3mA
Frame Frequency	Fclk	-	65	-	Hz	FR=65Hz setting
Standby Current	IDD1	-	-	1	uA	Display off, Oscillation off
Operating Current	IDD2	-	6	20	uA	VDD=3.3V, Ta=25 ℃, SR=00, FR=00, Frame inversion, FR=65Hz, with an LCD panel load.
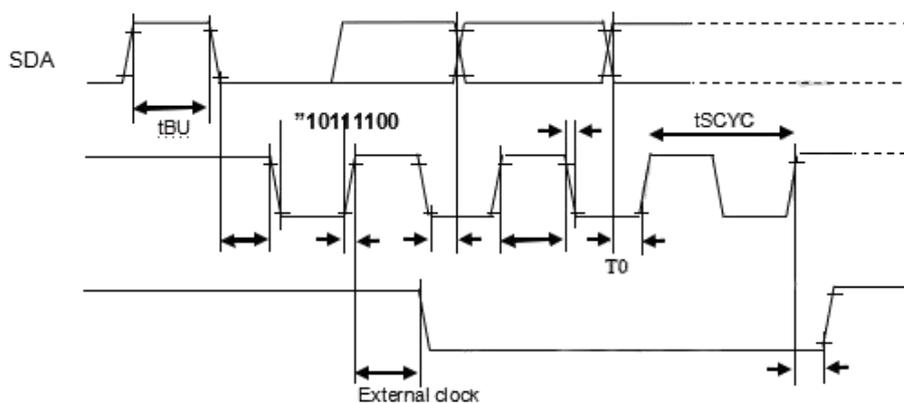
2-line serial interface timing

■ Equivalent circuit diagram of input and output terminal
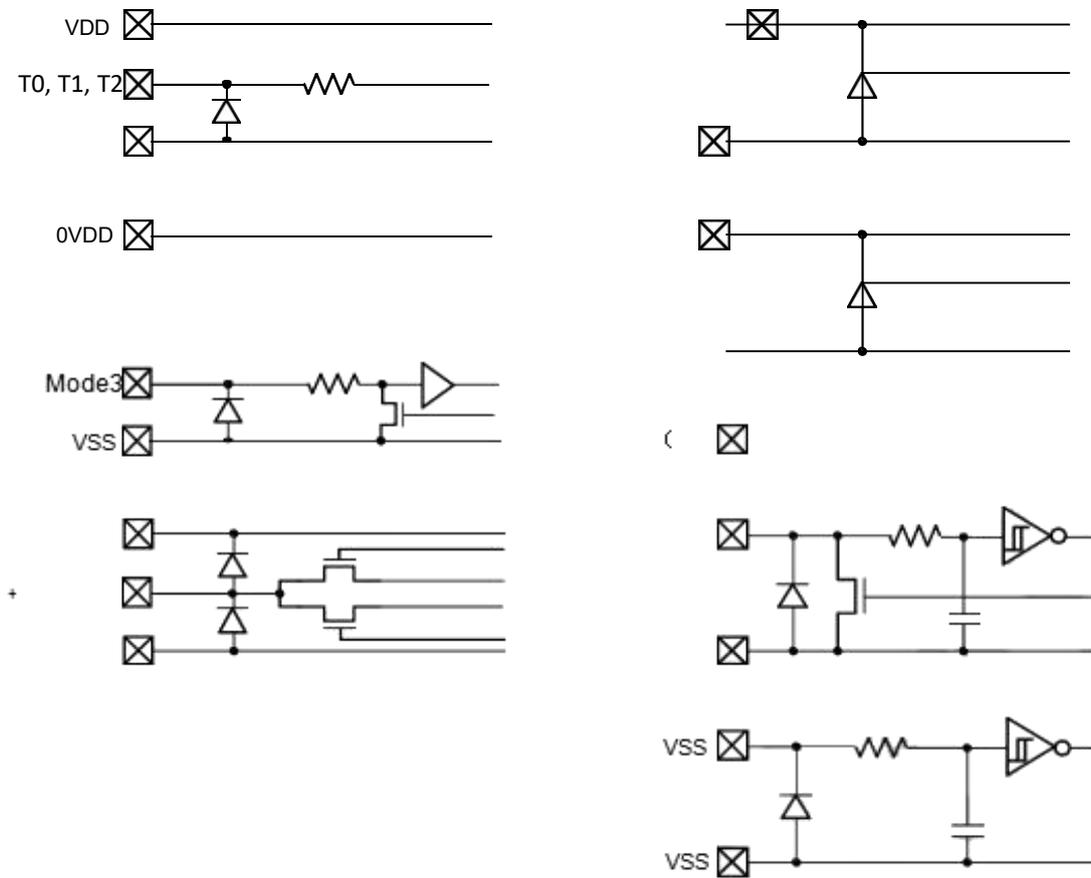
■ Command Registers Description

	7	6	5	4	3	2	1	0
ADSET	C	0	0	P[4:0]				
DISCTL	C	0	1	FR[1:0]		LF	SR[1:0]	
MODSET	C	1	0	ULP	EN	/	/	/
EVRSET	C	1	1	0	0	EV[3:0]		
ICSET	C	1	1	0	1	P[5]	RST	/
BLKCTL	C	1	1	1	0	BF[2:0]		
APCTL	C	1	1	1	1	EV[4]	AON	AOF

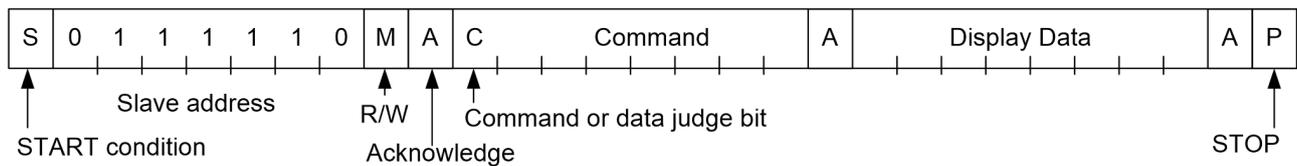| Name	Default	Description
P[5:0]	000000	DDRAM Address. In the write mode, the range of address P [5:0] can be set as 0~23(Hex). In the read mode, the range of address P [5:0] can be set as 0~23(Hex). Don't specify another address; otherwise address will be set to "000000". Note: The bit P[5] is in the command 'ICSET'.
FR[1:0]	00	Set Frame Frequency for Power Saving. 00, 65Hz, Normal Mode 01, 92Hz Power Save Mode1 10, 46Hz, Power Save Mode2 11, 130Hz, Power Save Mode3
LF	0	Set Line or Frame inverse mode. 0, Line inverse 1, Frame inverse
SR[1:0]	10	Set internal bias current for Power Saving. 00, *0.5 01, *0.67 10, *1.0, default value. 11, *1.8
ULP	0	Set '1' to enable the Ultra-Low-Power mode, which can decrease total power consumption further more along with 'SR' and 'FR' Power Save Mode.
EN	0	0: disable all blocks on-chip, all com/seg pin will be pulled to GND. 1: enable
EV[3:0]	0000	Adjust resistor divider for LCD contrast setting. 0000, 1.000 * (VDD-VLCD) 0001, 0.975 * (VDD-VLCD) 0010, 0.950 * (VDD-VLCD) 0011, 0.925 * (VDD-VLCD) 0100, 0.900 * (VDD-VLCD) 0101, 0.875 * (VDD-VLCD) 0110, 0.850 * (VDD-VLCD) 0111, 0.825 * (VDD-VLCD) 1000, 0.800 * (VDD-VLCD) 1001, 0.775 * (VDD-VLCD) 1010, 0.750 * (VDD-VLCD) 1011, 0.725 * (VDD-VLCD) 1100, 0.700 * (VDD-VLCD) 1101, 0.675 * (VDD-VLCD) 1110, 0.650 * (VDD-VLCD) 1111, 0.625 * (VDD-VLCD) Note: The bit EV[3] is in the command 'APCTL'.
RST	0	Set '1' to reset all the registers in this table, but it won't reset the display data in the DDRAM.
BF[2:0]	000	Config the blink frequency: 000, No blink. 001, 0.3Hz 010, 0.25Hz 011, 2Hz 100~111, 1Hz
AON: AOFF	00	Config the pixel display 00, All pixels are ON/OFF depending on the data in the display DDRAM. 01, All pixels are OFF regardless of DDRAM data. 10, All pixels are ON regardless of DDRAM data. 11, All pixels are OFF regardless of DDRAM data, the same as '01'.

■ Function Description

● Command and Data Transfer Method

The device transmits data through a two-wire serial interface. when a command or data is input through a two-wire serial interface, the start condition and stop condition states must be generated. when setting sda 'h' → 'l' on scl 'h', it becomes "start condition". When setting sda 'l' → 'h' on the scl 'h', it becomes the "stop condition ".
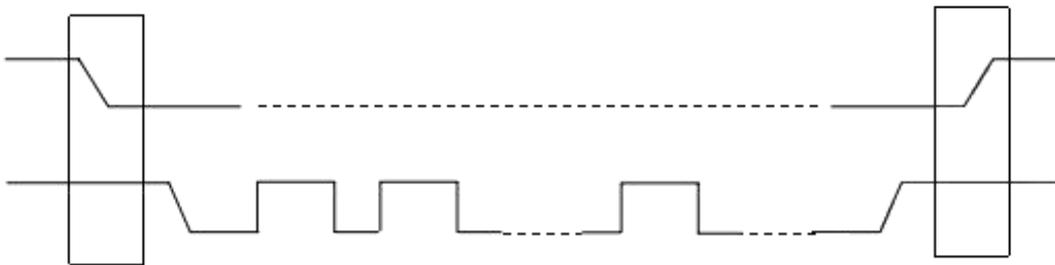
1. Generate "START condition".
2. Issue Slave address 7C.
3. Transfer command.
4. Transfer display data.
5. Generate "STOP condition"

| S | 0 | 1 | 1 | 1 | 1 | 1 | 0 | M | A | C | Command | A | Display Data | A | P |

START condition · Slave address · R/W · Acknowledge · Command or data judge bit · STOP

After generating the start condition, Command transfer (command transfer) handles the slave address in "01111100", The read mode is "01111101"). command input after the slave address. from the lowest valid bit (lsb) of the address determines whether the operation to be performed is a write operation or a read operation. msb (command or data judgment bit) defines whether subsequent bytes are commands or data. When command or data judgment bit 1, And the next byte is command. when "command or data judgment bit " "0", The next byte is the display data.

| Slave address | 1 Command | 1 Command | 1 Command | 0 Command | Display Data |

Once in the display data transfer state, no commands can be entered. To re-enter the command, regenerate the "start condition ".

If a "start condition" or "stop condition" is entered during instruction transfer, the instruction will be cancelled. if the slave address is continuously entered after the start condition, it will be in the command input state. please enter "slave address" in the first data transfer after "start condition ".

* When the slave address in the first data transfer can not be identified, the reply does not return and the next transmission will not be valid. When the data transfer is in an invalid state and the start condition is transmitted again, it returns to a valid state.

* Please observe the microprocessor interface characteristics for input rise time and set time and hold time while transmitting commands and data (see the microprocessor interface).

● Write Display Data and Transfer Method

Set R/W bit to '0' to come into write mode.

This device has Display Data RAM (DDRAM) of 36×4=144 bit.

DDRAM address

BIT		00	01	02	03	04	05	06	07	……	21H	22H	23H	
	0	a	e	i	m									COM0
	1	b	f	j	n									COM1
	2	c	g	k	o									COM2
	3	d	h	l	p									COM3
		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	……	SEG33	SEG34	SEG35	

8-bit data will be stored in DDRAM. The address to be written is the address specified by Address set command, and the address is automatically incremented in every 4bit data. Data can be continuously written in DDRAM by transmitting Data continuously.

	Slave address			Command		Command														
S	0111110	0	A	1	1101000	A	0	0000000	A	a b c d e f g h	A	i j k l m n o p	A	…	P

R/W=0(Write Mode)   → Display Data

● Read Command Register and Transfer Method

The command registers can be read during read mode. The sequence for the command registers reading is shown below and is similar to the display data reading sequence.

	Slave address			Command		Command			Slave address					
S	0111110	0	A	1	1101100	A	ADSET	A	S	0111110	1	A	Data	NA	P

R/W ↑   Set ICSET[P2]=1 ↑   R/W ↑

The command register addresses are described below. The following register settings can be read in this mode.

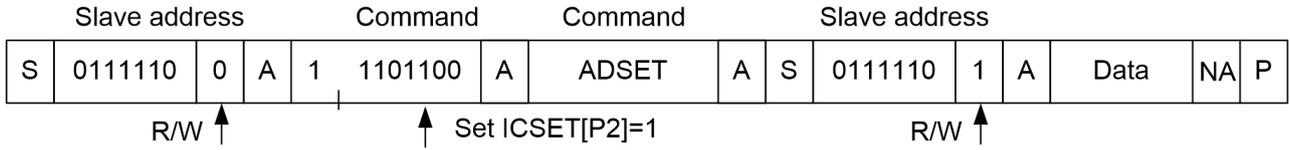| Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	/	/	/	/	RST	BF[2:0]			24H
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOF	25H
REG3	/	/	/	ULP	EV[3:0]				26H

● Frame inversion mode

● Read Command Register and Transfer Method

The command register can be read in the read mode. The reading order of the command register is as follows, which is similar to the reading order of the display data
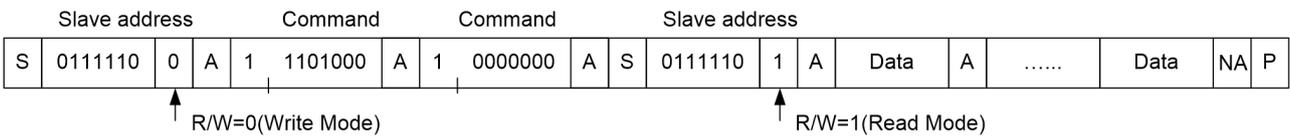
	Slave address			Command			Command		Slave address					
S	0111110	0	A	1 1101100	A	ADSET	A	S	0111110	1	A	Data	NA	P

R/W ↑   ↑ Set ICSET[P2]=1   R/W ↑

The command register address is as follows. The following register settings can be read in this mode.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	/	/	/	/	RST	BF[2:0]			24H
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOF	25H
REG3	/	/	/	ULP	EV[3:0]				26H

● Read Display Data and Transfer Method

The read mode sequence is shown below

	Slave address			Command			Command			Slave address				Data				Data		
S	0111110	0	A	1	1101000	A	1	0000000	A	S	0111110	1	A	Data	A	……		Data	NA	P

↑ R/W=0(Write Mode)   ↑ R/W=1(Read Mode)

An example of the display data read sequence is shown below.

■ TSSOP48 Package

12. 5±0. 1
(MAX12. 85 include. BURR)

48   25

8. 1±0. 2   6. 1±0. 1

1

0. 5   1PIN MARK   24

4° +6°
   -4°

0. 5±0. 15   1. 0±0. 2

0. 17 +0. 05
     -0. 03

S

1. 0MAX

0. 85±0. 05   0. 08±0. 08

0. 5   ⌴ 0. 08 S   0. 22 +0. 05 -0. 04   ⊕ 0. 08 Ⓜ

(UN I T : mm)